Abstract of the Disclosure

A synchronous flash memory includes an array of non-volatile memory cells. The memory array is arranged in rows and columns, and can be further arranged in addressable blocks. Data communication connections are used for bi-directional data communication with an external device(s), such as a processor or other memory controller. In one embodiment a non-volatile synchronous memory device includes an array of memory cells arranged in a plurality of addressable banks. A bank buffer circuit is coupled to each of the banks. Each of the buffers can store data from a row of memory cells contained in a corresponding bank. A method of operating a synchronous flash memory includes storing instruction code in each array block and copying the instruction code from a first array block to a buffer circuit, during a write operation, so that the instruction code can be read from the buffer circuit during the write operation.